Q8RF SPECIFICATIONS

FEATURE HIGHLIGHTS

INDUSTRY-LEADING PERFORMANCE

The Q8RF extends the capability of Xiphos' Q-Card line with an embedded multi-channel RFSoC (RF System On Chip). Like other Q-Cards, it provides a heterogeneous compute architecture including full ARM processing subsystem and extensive FPGA fabric. The Q8RF adds complete analog/digital programmability across the RF signal chain including 8x RF ADC @ 4 GSPS and 8x DAC @ 6.5 GSPS.

LOW MASS, VOLUME, POWER

The Q8RF measures 100 mm x 100 mm x 20 mm and consumes as little as 6.6 W. Its small size, low mass and power consumption make the Q8RF ideal for multi-channel RF applications that demand extremely high performance.

INTEGRATED HYBRID ENVIRONMENT

The Q8RF provides a tight integration of RF ADC and DACs, a quad core ARM Cortex A53 Application Processing Unit, a dual core ARM Cortex R5 Real Time Processing Unit, and massive programmable logic resources for application-specific use.

FLEXIBLE INTERFACING

The Q8RF provides 8x RF ADC @ 4 GSPS and 8x DAC @ 6.5 GSPS, external Ref Clock(s) Inputs, and a Ref Clock Output through its RF mezzanine connector.

The Q8RF also provides multiple digital I/O lines, including 1.8V/3.3V GPIO, LVDS, 28.21 Gbps GTY transceivers supporting PCIe Gen 3 & 100G Ethernet, and GTR transceivers supporting PCIe Gen 2 & SATA through its digital mezzanine connector.

APPLICATIONS

The extremely high performance and extensive FPGA fabric and RF ADCs/DACs make the Q8RF ideally suited for onboard:

- Multi-band advanced Software Defined Radios (SDR)
- Broadband Comms
- IoT
- Digital Beamforming Networks
- Synthetic Aperture Radar (SAR)
- RF Monitoring & Signal Intelligence (SIGINT)

PRODUCT INTEGRATION MODULE (PIM)

Each Q8RF is delivered with a detachable PIM to facilitate development. The PIM provides standard commercial interfaces (e.g. JTAG, USB), and other lab development features.

SOFTWARE DEVELOPMENT

Xiphos provides an Application Development Kit with standard Linux libraries for C/C++ to support software development on Linux workstations. Code previously developed for Linux desktop and server applications can be easily ported to the Q8RF. Q8RF hardware and logic interfaces are all accessible through either standard Linux and Xilinx kernel drivers or custom drivers provided by Xiphos.

LOGIC DEVELOPMENT

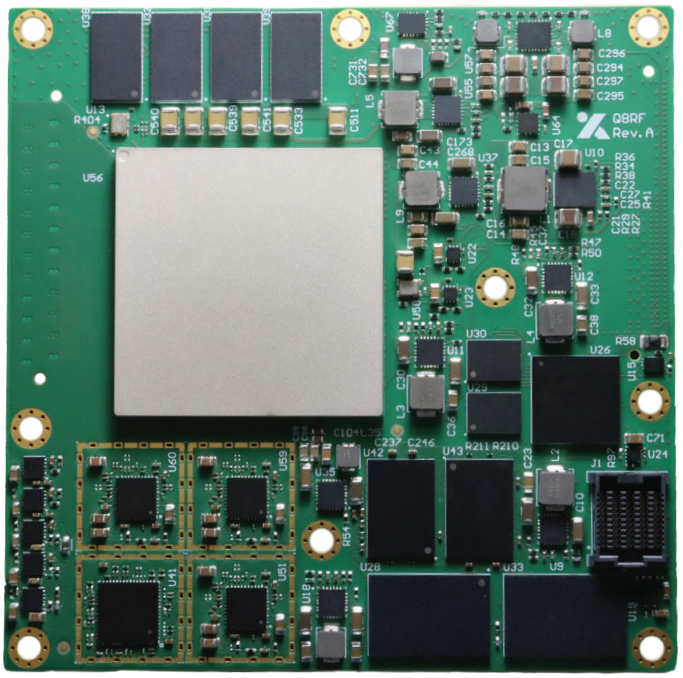
Logic development uses standard Xilinx development tools. Xiphos, Xilinx and many third party vendors also provide a wide range of compatible reusable logic cores for Xilinx FPGAs.

FLIGHT HERITAGE

The Q8RFS, the Flight Model (FM) version of the Q8RF, is awaiting first launch in 2024:

Other flight heritage products in the current Xiphos Q-Card family include the Q7S, Q8S, and Q8JS.

Over 200 Q-Cards have flown to date
Xiphos has been flying previous generations of the Xiphos Q-Card family since 2002.



CHARACTERISTICS

MEMORY
- 4 GB PS DDR4 DRAM (with EDAC)
- 4 GB PL DDR4 DRAM
- 2x 256 MB QSPI Flash (NOR)
- 2x 32 GB NAND Flash

MULTI PROCESSOR SYSTEM ON CHIP
- Xilinx UltraScale+ ZU28DR RFSoC
- Quad-core ARM Cortex A53 Application Processing Unit at up to 1.2 GHz
- Dual-core ARM Cortex-R5 @ 500 MHz
- 8x RF ADC @ 4 GSPS
- 8x DAC @ 6.5 GSPS
- 930,000 system logic cells
- 850,000 flip-flops (FF)
- 425,000 lookup tables (LUT)
- 4,272 DSP slices

CONTROL FPGA
- Microchip ProASIC3

OPERATING SYSTEM
- Yocto Linux BSP (LTS distribution)

FORM FACTOR
- 100 mm x 100 mm x 20 mm, <200 g (without connectors)

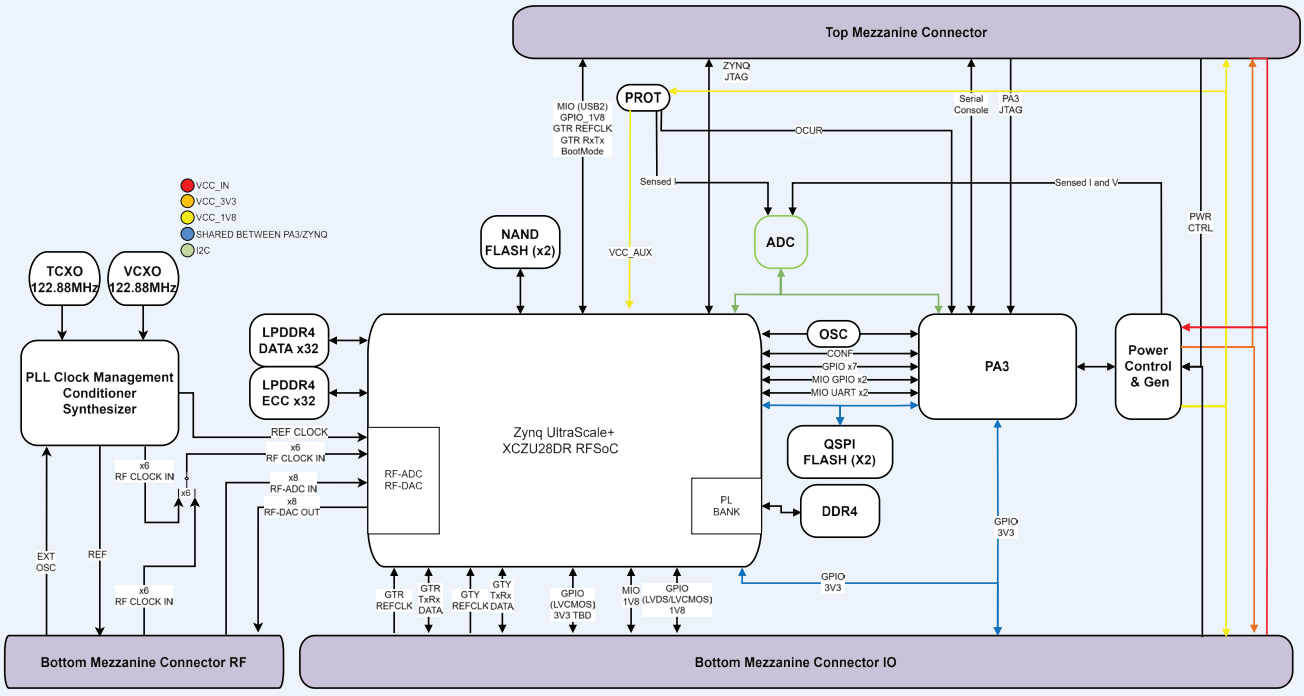
ENVIRONMENTAL
- Operating Temperature -40 to +60C

INTERFACES
- RF Mezzanine Connector
- 8x Transmit + 8x Receive RF
- Ext Ref Clock(s) In, Ref Clock Out

I/O BOTTOM MEZZANINE CONNECTOR
- 46x LVDS or 92x 1.8V GPIO, 39x 3.3V GPIO
- 16x 28.21 Gbps GTY transceivers supporting PCIe Gen 3 & 100G Ethernet
- 3x GTR transceivers supporting PCIe Gen 2 & SATA

Q8RFS FLIGHT MODEL INCLUDES
- Triple mode redundancy in Control FPGA
- EDAC-protected RAM
- Upset and multi-current monitoring
- Overcurrent protection (multiple)
- FPGA bit-stream scrubbing
- Software robustness / watchdog
- 30krad TID lifetime

BLOCK DIAGRAM



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