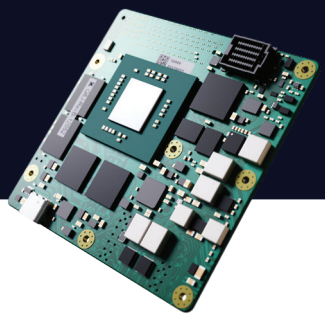


Q8J SPECIFICATIONS

FEATURE HIGHLIGHTS

INDUSTRY-LEADING PERFORMANCE

The Q8J features a Multi-Processor-System-on-Chip (MPSoC), including multi-core CPUs providing 64 bit processor scalability supported by programmable logic resources and a wide array of hardware interfaces.

LOW MASS, VOLUME, POWER

The Q8J measures 80 mm x 80 mm x 11.2 mm and consumes as little as 5 W. Its small size, low mass and power consumption make the Q8J ideal for aerospace applications that demand extremely high performance.

INTEGRATED HYBRID ENVIRONMENT

The application space in a Q8J is a tight integration of a quad core ARM Cortex A53 Application Processing Unit, a dual core ARM Cortex R5 Real Time Processing Unit, an ARM Mali 400 GPU and programmable logic, featuring 504,000 system logic cells, 461,000 flip flops, 274,000 lookup tables and 1,728 DSP slices reserved for application specific use.

OVERVIEW

The Q8J extends the capability of the Xiphos Q8 processor, adding support for high-speed JESD204B interfaces and PCIe, as well as access to external DDR3 or DDR4 memory. The Q8J is ideal for advanced SDR applications, I/O-intensive payload processing, and high-speed C&DH systems. At the core of each Q8J is a hybrid environment of powerful multi-core CPUs and reprogrammable logic, providing flexible and scalable performance.

FLEXIBLE INTERFACING

The Q8J provides Gigabit Ethernet networking through its RJ45 connector along with a USB 2.0/USB 3.1 Gen 1 Host port. The Q8J also provides multiple digital I/O lines, including up to 76 single-ended GPIO, 12 MIO, 50 LVDS pairs/100 single-ended GPIO, 17 Gigabit transceivers (full duplex) +5 clock references, USB 2.0 and factory-selectable RS-232/422/485 through its mezzanine connector. The Gigabit transceivers can support JESD204B to interface with high speed ADCs, DACs and RF transceivers, as well as PCIe.

APPLICATIONS

The extremely high performance and extensive FPGA fabric make the Q8J ideally suited for onboard:

- High resolution camera interfacing and control
- Onboard image processing
- Synthetic Aperture Radar (SAR) processing
- Hyper/multispectral compression
- Image registration and alignment
- Mass memory applications
- Convolutional neural networks
- Advanced wideband Software Defined Radios (SDR)

PRODUCT INTEGRATION MODULE (PIM)

Each Q8J is delivered with a detachable PIM to facilitate development. The PIM provides standard commercial interfaces (e.g. CAN, RS-232/422/485, 1-Wire, 13 GPIO, 8 analog inputs, 4 analog outputs, JTAG), debug LEDs and other lab development features.

SOFTWARE DEVELOPMENT

Xiphos provides an Application Development Kit with standard Linux libraries for C/C++ to support software development on Linux workstations. Code previously developed for Linux desktop andserver applications can be easily ported to the Q8J. Q8J hardware and logic interfaces are all accessible through either standard Linux and Xilinx kernel drivers or custom drivers provided by Xiphos.

LOGIC DEVELOPMENT

Logic development uses standard Xilinx development tools. Xiphos, Xilinx and many third party vendors also provide a wide range of compatible reusable logic cores for Xilinx FPGAs.

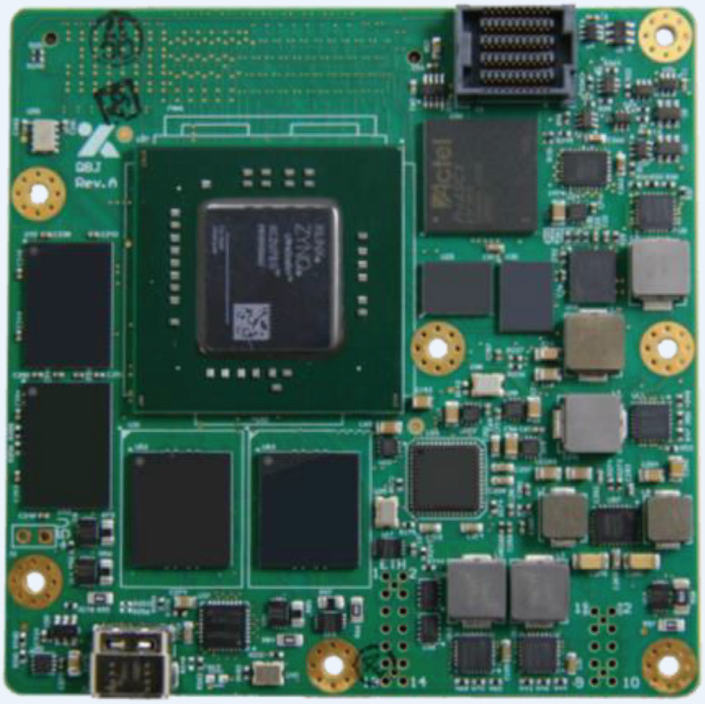
FLIGHT HERITAGE

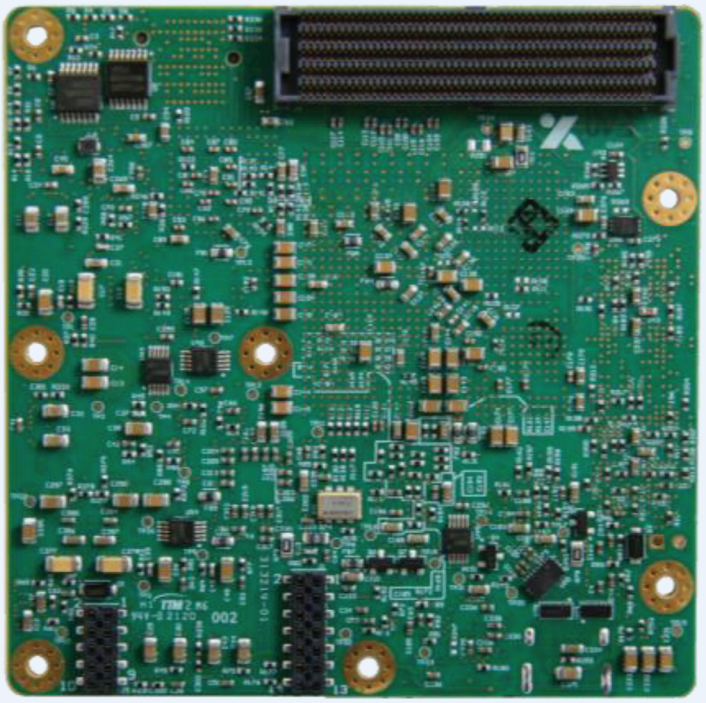
The Q8JS, the Flight Model (FM) version of the Q8J, has been flying since January 2023:

Other flight heritage products in the current Xiphos Q-Card family include the Q7S and Q8S.

Xiphos has been flying previous generations of the Xiphos Q-Card family since 2002

FRONT & BACK





CHARACTERISTICS

MEMORY
- 4 GB LPDDR4 DRAM
- 2x 256 MB QSPI Flash (NOR)
- 2x eMMC, 128 GB each, on independent buses / power control
- External PL-accessible DDR3 or DDR4 DRAM

MULTI PROCESSOR SYSTEM ON CHIP
- Xilinx Zynq UltraScale+ XCZU7EG
- Quad-core ARM Cortex A53 Application Processing Unit at up to 1.2 GHz
- Dual core ARM Cortex R5 Real Time Processing Unit at up to 500 MHz
- ARM Mali-400 GPU at up to600 MHz
- 504,000 system logic cells
- 461,000 flip-flops (FF)
- 274,000 lookup tables (LUT)
- 1,728 DSP slices

CONTROL FPGA
- Microchip ProASIC3

OPERATING SYSTEM
- Yocto Linux BSP (LTS distribution)

REAL TIME CLOCK
- RTC with sleep & wake up on alarm/interrupt
- Dedicated power pin for external battery

FORM FACTOR
- 80 mm x 80 mm x 11.2 mm, 56 g (without connectors)

POWER
- 5 W, typical
- 6 to 16 VDC
- Various power modes (including deep sleep)
- Overcurrent detection & protection (global and local) and brownout protection and local) and brownout protection

ENVIRONMENTAL
- Operating Temperature -40 to +60C

INTERFACES
- Power
- Gigabit Ethernet (RJ45 on adapter)
- 1x USB Type-C Host port (USB 2.0 & USB 3.1 Gen 1)
- CAN Bus & PCIe controllers (in logic)
- Up to 25 single-ended GPIO 3.3 V, 51 single-ended GPIO 1.8 V, 12 MIO 1.8 V, 50 LVDS pairs/100 single-ended GPIO 1.8 V, 16 PL GTH transceivers (up to 12.5 Gbps for JESD204B, PCIe) + 4 clock references, 1 PS GTR transceiver (up to 6 Gbps, for SATA, PCIe), USB 2.0, and factory-selectable RS-232/422/485 (Mezzanine connector)

Q8JS FLIGHT MODEL INCLUDES
- Triple mode redundancy in Control FPGA
- EDAC-protected RAM
- Upset and multi-current monitoring
- Overcurrent protection (multiple)
- FPGA bit-stream scrubbing
- Software robustness / watchdog

xiphos.com
sales@xiphos.com

3981 St-Laurent Boulevard, Suite 500,
Montreal, Quebec, H2W 1Y5, Canada

XIPHOS